ABSTRACT OF THE DISCLOSURE

A sequence control circuit that is capable of operating at high-speed without using either a memory having a short access time or high-speed devices is provided. Each address of an instruction memory includes an instruction next to the current instruction designated by a program counter signal and an instruction of the jump target of the current instruction. Instruction registers receive instructions from the instruction memory to output those in the next cycle. A selector selects either one of the outputs from the instruction registers depending on a jump signal. A program counter control section decodes an instruction from the selector to determine the next program counter signal and a jump signal. An address register receives the next program counter signal to output an instruction memory address in the next cycle. A jump register receives the jump signal to output that to the selector in the next cycle.